Specification
GAYLE
Gate array for A300/A500++

1.0 DESCRIPTION

GAYLE is a gate array IC used in the A300 and related systems. It is packaged in an 84 pin plastic leaded chip carrier (PLCC) whose pinout is shown below. GAYLE is capable of operating a 68000 based Amiga computer with theECS chipset, and a processor clock speed of 7.16 Mhz. GAYLE provides the following functions:

- Address decoding and timing for system ROM
- Address decoding and timing for optional flash ROM
- Address decoding and timing for chip RAM
- Address decoding and timing for chip registers
- Address decoding and timing for 8520's (CIA's)
- Address decoding and timing for real time clock (RTC)
- Address decoding and timing for Credit card connector
- Address decoding and timing for IDE hard disk drive
- Address decoding and timing for COM200020 ArcNet chip
- Generation of ECLK clock signal
- Data buffer control
- System RESET logic
- Floppy glue

{Insert pinout here}

1.1 CONFIGURATION

The device shall be configured as a standard 84 pin plastic leaded chip carrier with external dimensions as shown in Figure XX-x. Refer to figure x-x for connection diagram.

1.2 SOURCES

Refer to Approved Vendor List.

1.3 PIN DESCRIPTIONS

NUM	CLASS	NAME	DESCRIPTION
1	OUT	PE12	Program Voltage 12V Enable
2	OUT	PE5	Program Voltage 5V Enable
3	PWR	Gnd1	Ground
4	TS	NOISE	Digital Audio
5	OUT	_CC_RESET	Memory Card Reset
6	OUT	_CC_ENA	Memory Card Enable
7	OUT	_REG	Memory Card "Register" Space
8	OUT	_CEL	Memory Card Chip Enable Low byte
9	OUT	_CEU	Memory Card Chip Enable High byte
10	OUT	_FLASH_CEL	Flash Memory Chip Enable Low
11	OUT	_FLASH_CEU	Flash Memory Chip Enable High
12	IN	_IDE_IRQ	IDE Drive Interrupt Request
13	OUT	_IDE_CS(1)	IDE Drive Chip Select 1
14	OUT	_IDE_CS(2)	IDE Drive Chip Select 2
15	OUT	_SPARE_CS	Spare Chip Select
16	OUT	_NET_CS	Network Controller Chip Select
17	OUT	_RTC_CS	Real Time Clock Chip Select
18	OUT	_IOWR	I/O Write Strobe
19	OUT	_IORD	I/O Read Strobe
20	PWR	Vcc1	+5V
21	OUT	_ROMEN	ROM Chip Enable
22	IN	C14M	14 MHz Clock In (master)
23	IN	CCK	CCK Clock IN (sync)
24	PWR	Gnd2	Ground
25	IN	XRDY	Expansion Bus Wait
26	IN	_OVR	Expansion Bus Decode Override
27	OC	_OEL	Chip->68000 Bus Buffer Enable
28	OC	_OEB	68000->Chip Bus Buffer Enable
29	IN	_DBR	Agnus Chip Data Bus Required
30	OUT	_BLS	Agnus Chip Blitter Slowdown
31	OUT	_REGEN	Agnus Chip Register Enable
32	OUT	_RAMEN	Agnus Chip RAM Enable
33	IN	_AS	68000 Address Strobe
34	IN	_UDS	68000 Upper Data Strobe
35	IN	_LDS	68000 Lower Data Strobe
36	IN	R_W	68000 Read/Write
37	TS	_DTACK	68000 Data Transfer Acknowledge
38	IN	_BGACK	68000 Bus Grand Acknowledge
39	OC	_HLT	68000 Halt
40	OC	_RST	68000 Reset
41	OUT	E	CIA Phi 2
42	IN	A12	68000 Address Bit 12
43	IN	A13	68000 Address Bit 13
44	IN	A15	68000 Address Bit 15
45	PWR	Gnd3	Ground
46	IN	A16	68000 Address Bit 16
47	IN	A17	68000 Address Bit 17
48	IN	A18	68000 Address Bit 18
49	IN	A19	68000 Address Bit 19
50	IN	A20	68000 Address Bit 20

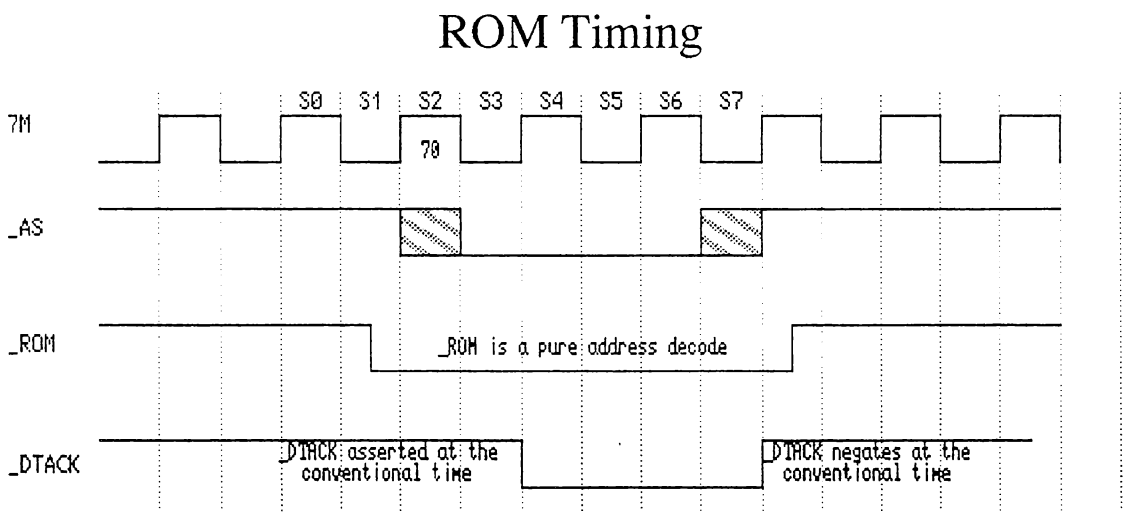
51	IN	A21	68000 Address Bit 21
52	IN	A22	68000 Address Bit 22
53	IN	A23	68000 Address Bit 23
54	IO	D7	68000 Data Bit 7
55	IO	D6	68000 Data Bit 6
56	IO	D5	68000 Data Bit 5
57	IO	D4	68000 Data Bit 4
58	IO	D3	68000 Data Bit 3
59	IO	D2	68000 Data Bit 2
60	IO	D1	68000 Data Bit 1
61	IO	D0	68000 Data Bit 0
62	PWR	Vcc2	+5V
63	IN	_KBRESET	Keyboard Reset In
64	OUT	DKWEB	Floppy Write Enable Out
65	OUT	DKWDB	Floppy Write Data Out
66	PWR	Gnd4	Ground
67	OUT	MTRON	Floppy Motor On Out
68	OUT	MTRX	Floppy Motor Out
69	IN	DKWE	Floppy Write Enable In
70	IN	_DKWD	Floppy Write Data In
71	IN	_MTR	Floppy Motor In
72	IN	_SEL	Floppy Select In
73	OUT	_ODD_CIA	CIA Odd Chip Select
74	OUT	_EVEN_CIA	CIA Even Chip Select
75	IN	_CC_CD(1)	Memory Card Card Detect 1
76	IN	_CC_CD(2)	Memory Card Card Detect 2
77	IN	_CC_BVD(1)	Memory Card Battery Voltage Detect 1
78	IN	_CC_BVD(2)	Memory Card Battery Voltage Detect 2
79	IN	_CC_WP	Memory Card Write Protect
80	IN	_CC_BUSY_IREQ	Memory Card Busy/Interrupt Request
81	IN	_WAIT	Memory Card Wait
82	OC	_BERR	Bus Error Interrupt Request
83	OC	_INT6	High Priority Interrupt Request
84	OC	_INT2	Low Priority Interrupt Request

2.0 SYSTEM ROM

The onboard ROMs are selected in the address range from $0A80000 to $0B7FFFF, $0E00000 to $0E7FFFF, and $0F80000 to $0FFFFFF. The ROMs are also selected in the range from $0000000 to $01FFFFF when the internal overlay signal (OVL) is high (this allows the RESET vectors to be contained in the ROMs). The internal OVL signal becomes asserted at reset, and negates on the first write to CIA1 (address range of $BFD000 to $BFDFFF.

2.1 ROM Timing

ROM timing is shown below:



3.0 FLASH ROM

There is provision for an optional flash ROM device. The intent is that this is a possible replacement for a floppy disk drive in an extremely low end variant of the A300. Two address decodes are provided, _CEL and _CEU, selecting the low and high bytes respectively. They are active in the address range from $0A00000 to $0A7FFFF. These outputs are enabled when the proper data strobe is asserted, and the address is in range. Generation of _DTACK is identical to that for system ROM accesses.

3.0 CHIP RAM

Chip RAM cycles are generated during accesses to locations $0000000 to $0200000. When the internal OVL signal is asserted, ROM appears in this space instead of chip RAM (see section on ROM for further information on OVL).

3.1 Chip RAM Timing

Timing for chip RAM cycles is given in the timing section of the Chip Register discussion (section 4.1). All timings given are equally valid for either chip registers or chip RAM.

4.0 CHIP REGISTERS

The chip registers are selected in the range from $0DFF000 to $0DFF1FF. Chip registers show up in user and supervisor data space.

4.1 Chip RAM and Register Timing

Timing is given on the following page. Note that timimng for chip RAM accesses is identical. A wait state is inserted when the access is from a DMA device (George??).

Chip RAM and Register Timing

{Insert timing diagram here}

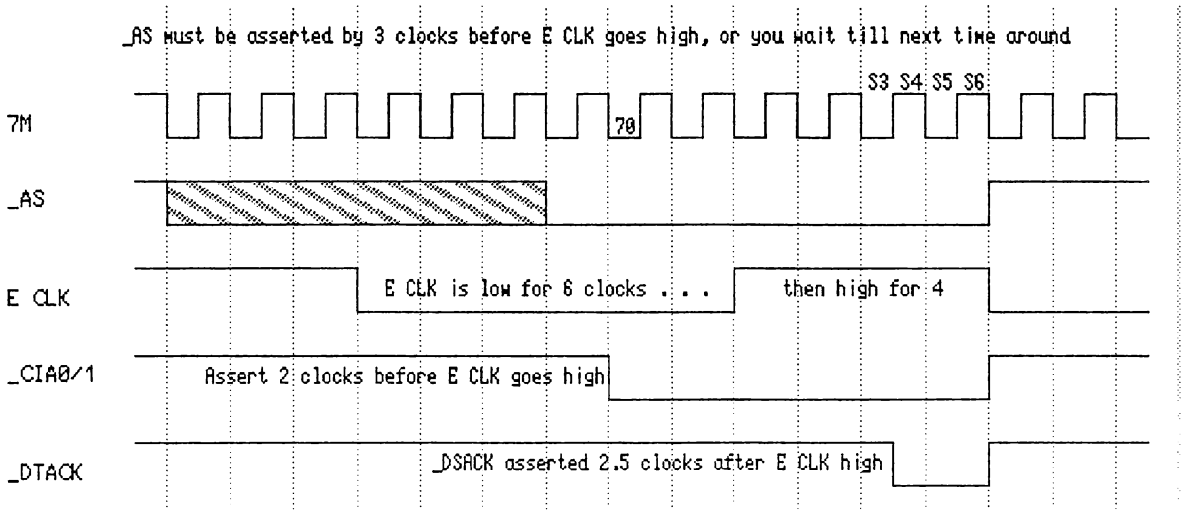
5.0 CIA's

The 8520 CIA's are selected in the address range from $0BF0000 to $0BFFFFF. CIA0 responds to addresses in this range in which address line 12 is low, with data appearing at odd addresses. The standard location to use in accesssing CIA0 is from $0BFE000 to $0BFEFFF. CIA1 responds to addresses from $0BF0000 to $0BFFFFF in which address line 13 is low, with data appearing at even addresses. The standard location to use for accessing CIA1 is from $0BFD000 to $0BFDFFF.

5.1 CIA timing

GAYLE provides synchronization of the processor to CIA accesses as well as generation of the E clock signal. Timing is shown below:

CIA Timing



6.0 REAL-TIME CLOCK

The internal real-time clock (RTC) is selected in the address range from $0DC0000 to $0DC7FFF if no external real time clock is present, or from $0DC8000 to 0DCFFFF if an external real-time clock is present. This arrangement is necessary to be able to support bridgeboards that plug into the A501 slot on A500++. The RTC appears in both user and supervisor spaces.

6.1 RTC Timing

The real-time clock timing is based on the Ricoh RP5C01 real-time clock chip. GAYLE's timing to the RTC is shown below:

Real Time Clock Timing

{Insert timing diagram here}

7.0 IDE HARD DRIVE

The IDE (AT) hard drive requires two mutually exclusive chip selects. Please see the chart below for address range in which each is active. The _IOW and _IOR signals have timing that is valid for IDE hard drives during these cycles.

Data register accesses can be performed faster than control register accesses. Accesses to the control registers are called "8 bit accesses" while those to the data register are called "16 bit accesses". Shown below is a table that gives the chip select and access speed versus address range.

A13	A12	Address Range	Chip Select	Speed
0	0	$0DA0000 to $0DA0FFF	_CS1	8 bit
0	1	$0DA1000 to $0DA1FFF	_CS2	8 bit
1	0	$0DA2000 to $0DA2FFF	_CS1	16 bit
1	1	$0DA3000 to $0DA3FFF	_CS2	16 bit

7.1 IDE Timing

IDE timing is shown below:

IDE Drive Timing

{Insert timing diagram here}

7.3 IDE Register Map

The disk drive address lines DA0, DA1, and DA2 are expected to be connected to processor address lines A2, A3, and A4 respectively. When connected in this fashion, the following memory map results:

Addr on A1000+	Addr on AT	Valid Data	Read Function	Write Function
$0DA0018	3F6	8 bits	Alternate Status	Device Control
$0DA001C	3F7	8 bits	Drive address	Not used
$0DA1004	1F1	8 bits	Error Register	Features
$0DA1008	1F2	8 bits	Sector Count	Sector Count
$0DA100C	1F3	8 bits	Sector Number	Sector Number
$0DA1010	1F4	8 bits	Cylinder Low	Cylinder Low
$0DA1014	1F5	8 bits	Cylinder High	Cylinder High
$0DA1018	1F6	8 bits	Drive/Head	Drive/Head
$0DA101C	1F7	8 bits	Status	Command
$0DA2000	1F0	16 bits	Data	Data

8.0 ARCNET

A chip select is provided for an SMC COM20020 ARCNET chip. The COM20020 interfaces directly to the processor for all other signals.

8.1 ArcNet Timing

Timing for the SMC COM20020 is shown below:

ArcNet Timing

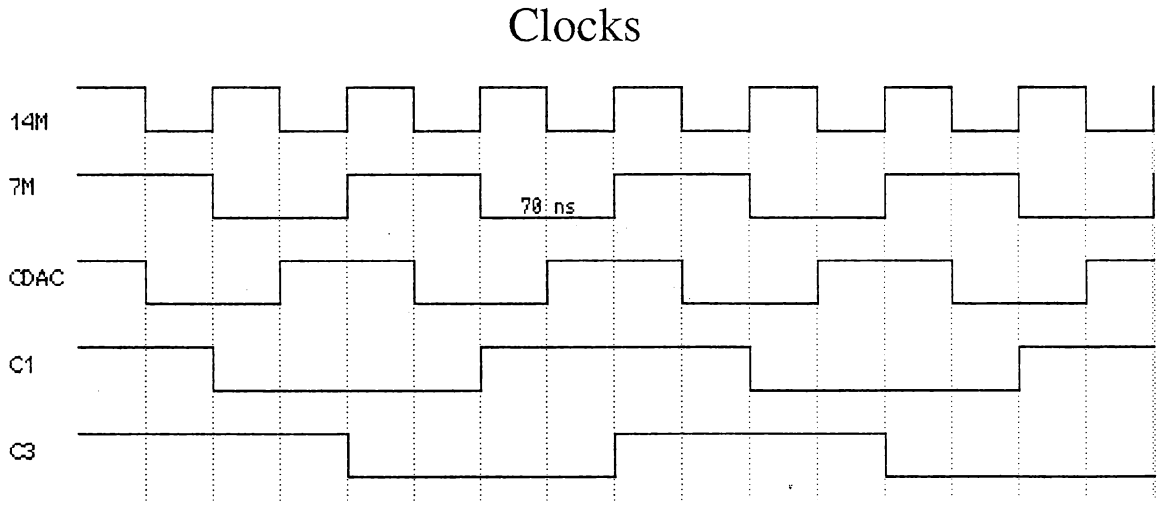
{Insert timing diagram here}

10.0 SYSTEM RESET LOGIC

The _KBRESET input drives the open collector outputs _RESET an d _HALT low. When _RESET and _HALT are externally driven low, all internal states in GAYLE are reset.

11.0 SYSTEM CLOCKS

The system clocks expected by ANIMAL are shown below. Note that C3 is generated internally.



12.0 FLOPPY GLUE

The floppy signals _MTRON, _MTRX, _DKWDB, and _DKWEB are generated by GAYLE. All of these signals are open collector outputs.

_MTRON is the signal that tells the floppy motor to turn on. It is the _MTR input latched by the _SEL input. _MTRON is guaranteed negated when _RESET is asserted.

_MTRX is the signal that tells the floppy motor to do what, George? It follows the _ MTR input except during reset when it is guaranteed negated.

_DKWDB is a buffered version of the _DKWD signal.

_DKWEB follows DKWE, except it is negated during reset.

13.0 BUFFER CONTROL

SHould this be folded in with other sections, or is there something special to say, George?

14.0 DTACK GENERATION

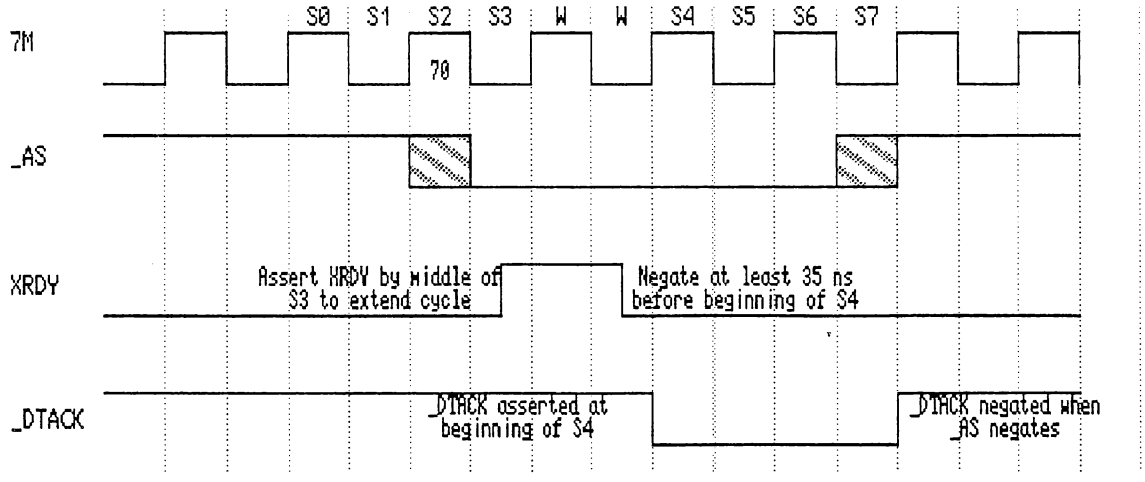
Automatic generation of the 68000 cycle termination signal, DTACK, is provided. GAYLE decodes addresses to determine timing for the DTACK signal. Timing for DTACK is given in many of the individual sections of this specification, but for any address ranges not covered in other sections (such as expansion space), DTACK works as follows:

1. If _OVR or XRDY are not asserted, DTACK is generated at the beginning of S4, guaranteeing a 4 clock cycle.
2. When _OVR is asserted, the _DTACK output is tristated, allowing the device that asserted _OVR to generate its own _DTACK.
3. If XRDY is asserted in time, generation of _DTACK is held off until XRDY is negated.

14.1 DTACK Timing

Timing for DTACK is shown below:

DTACK Timing



15.0 OVR SIGNAL

In addition to its function in overriding the generation of _DTACK, the _OVR signal can override address decoding in GAYLE. Thus it can be used to allow external devices to reside in address ranges that are normally reserved for motherboard devices, such as the credit card interface. Use of _OVR for this use basically requires that _OVR is asserted earlier than _AS. Address ranges where this is effective are shown below:

Address range	Normal cycle type	Cycle type with _OVR
$400000 -$7FFFFF	Credit card memory	Zorro II
$800000 -$8FFFFF	Credit card attributres	Zorro II
$900000 -$9FFFFF	Credit card I/O	Zorro II
$A00000 -$A7FFFF	Flash ROM	Zorro II
$A80000 -$B7FFFF	Workbench ROM	Zorro II
$B80000 -$BEFFFF	Reserved for CDTV	Zorro II
$DB0000-$DB0000	External IDE drive	Zorro II
$DD0000-$DDFFFF	Reserved for DMA contr	Zorro II
$E00000 -$E7FFFF	System ROM	Zorro II
$F80000 -$FFFFFF	System ROM	Zorro II

16.0 CREDIT CARD INTERFACE

GAYLE includes a complete interface to the industry standard PCMCIA cartridge. Limited support of hot insertion and removal is included. What else is there to say?

Four registers are included that facilitate support of the cartridge slot:

addr	00/r	00/w	01/r	01/w	10/r	10/w	11/r	11/w	NOTES
reg	status read	status write	status change read	status change write	int enable read	int enable write	control read	control write	
bit									
15	IDE INT STATUS	na	IDE INT CHANGE	IDE INT CLEAR	IDE INT I.E.(2)	IDE INT I.E.(2)	PAGE 25	PAGE 25	(6,1,2)
14	CC DET STATUS	na	CC DET CHANGE	CC DET CLEAR	CC DET I.E.(6)	CC DET I.E.(6)	PAGE 24	PAGE 24	(1,2)
13	BVD2/DA STATUS	na	BVD2/DA CHANGE	BVD2/DA CLEAR	BVD* I.E.(2)	BVD* I.E.(2)	PAGE 23	PAGE 23	(1,2)
12	BVD1/SC STATUS	na	BVD1/SC CHANGE	BVD1/SC CLEAR	BVD* I.E.(6)	BVD* I.E.(6)	PAGE 22	PAGE 22	(1,2)
11	WR PROT STATUS	S/W PROT	WR PROT CHANGE	WR PROT CLEAR	BSY/IRQ I.E.(2)	BSY/IRQ I.E.(2)	SLOW MEM	SLOW MEM	(1,9)
10	BSY/IRQ STATUS	na	BSY/IRQ CHANGE	BSY/IRQ CLEAR	BSY/IRQ I.E.(6)	BSY/IRQ I.E.(6)	FAST IO	FAST IO	(1,9)
9	D.A. ENABLE	D.A ENABLE	RESET CC SC	RESET CC SC	ANY IRQ 2	na	PROGRAM 12V	PROGRAM 12V	(3,4,6,7)
8	CARD DISABLE	CARD DISABLE	BEER CC SC	BEER CC SC	ANY IRQ 6	na	PROGRAM 5V	PROGRAM 5V	(3,5,6)

Notes:

(1) Writing a 1 to the status write forces the condition to be always true. Writing a 0 to the status change write resets the status change flag.

(2) If the page facility is present, the page bits are read/write.

(3) Setting both programming voltages is defined to assert the credit card reset signal.

(4) Setting the RESET/CC SC bit enables a system reset when the credit card is inserted or removed.

(5) Setting the BEER/CC SC bit enable a bus error on the first access to the credit card space after a status change.

(6) If either the RESET or BEER SC bits is implemented, that bit is read/write.

(7) The D.A. (digital audio) ENABLE bit enables the BVD2/DA pin to drive the NOISE out pin and disables the BVD2/DA input to the BVD* interrupt.

(8) It is intended that the minimum IDE drive I/F uses bit 7 of the STATUS register to detect interrupts, implementing the IDE I.E. bit is optional since this function is duplicated in the drive.

(9) The SLOW MEM and FAST I/O bits force 1.2 uS memory cycles and 560 ns I/O cycles for the credit card memory and I/O areas.

17.0 MEMORY MAP

0000000 to 01FFFFF	2 MB	Chip RAM (or system ROM in overlay)
0200000 to 03FFFFF	2 MB	Zorro II expansion space
0400000 to 07FFFFF	4 MB	Credit Card memory if CC present (ZII otherwise)
0800000 to 08FFFFF	1 MB	Credit Card attributes if CC present (ZII otherwise)
0900000 to 09FFFFF	1 MB	Credit Card I/O if CC present (ZII otherwise)
0A00000 to 0A7FFFF	512 KB	Flash ROM
0A80000 to 0B7FFFF	1 MB	System ROM selected (optional workbench ROM)
0B80000 to 0BEFFFF	448 KB	Not used (Reserved for CDTV)
0BF0000 to 0BFFFFF	64 KB	CIA's (See section on CIA's for more detail)
0C00000 to 0D7FFFF	1.5 MB	C00000 Memory
0D80000 to 0D8FFFF	64 KB	Not used
0D90000 to 0D9FFFF	64 KB	ARCNET chip select
0DA0000 to 0DA7FFF	32 KB	IDE drive (see section on IDE for register map)
0DA8000to 0DAFFFF	32 KB	Credit Card & IDE configuration registers
0DB0000 to 0DBFFFF	64 KB	Not used (Reserved for external IDE)
0DC0000 to 0DCFFFF	64 KB	Real time clock
0DD0000 to 0DDFFFF	64 KB	RESERVED for DMA controller
0DE0000 to 0DEFFFF	64 KB	Not Used
0DF0000 to 0DFFFFF	64 KB	Chip registers (shadowed 8 times)
0E00000 to 0E7FFFF	512 KB	System ROM (1st half if 1MB ROM)
0E80000 to 0EFFFFF	512 KB	Configuration and I/O card space
0F00000 to 0F7FFFF	512 KB	Cartridge space
0F80000 to 0FFFFFF	512 KB	System ROM (2nd half if 1MB ROM)

18.0 PHYSICAL REQUIREMENTS

18.1 Marking

Devices shall be marked with Commodore part number plus a copyright notice as follows:
1990 CBM.

18.2 Packaging

The interconnected circuitry shall be contained in a standard 84-pin plastic leaded chip carrier with exterminal dimensions shown in Figure XX-X.

19.0 PROCESS QUALIFICATION TESTS

Integrated circuitrs supplied to the requirements of this specification shall meet the requiremtnes of Engineering Policy No. 1.02.008, whatever that is. Supporting doucmentation shall be supplied by vendor upon request.

19.1 Environmental test conditions

Devices shall comply with blah blah blah